IN THE CLAIMS:

1. (Previously Presented) In a microprocessor performing speculative instruction execution, a method comprising the steps of:

providing a structure to track register allocation for a first thread of said microprocessor; and

tracking a first set of pointers in said structure assigned to manage said register allocation for an instruction of said first thread of said microprocessor to prevent a register allocated as a destination operand for said instruction of said first thread from being overwritten before said instruction of said first thread retires, said first set of pointers includes at least two pointers set apart by a fixed distance and move in unison, at all times, up and down said structure.

2. (Previously Presented) The method of claim 1, further comprising the step of tracking a second set of pointers in said structure assigned to manage a register allocation for an instruction of a second thread of said microprocessor to prevent a register allocated as a destination operand for said instruction of said second thread from being overwritten before said instruction of said second thread retires, whereby said first set of pointers and said second set of pointers track independently of each other.

3. (Previously Presented) The method of claim 1, wherein said structure comprises pointers to said registers allocated and pointers to registers deallocated, where said registers allocated and said registers deallocated are physical registers that operate as a destination operand for said instructions executing on a multithreading microprocessor where said destination operands identifies where data resulting from logical operations are to be written.

4. (Previously Presented) The method of claim 1, wherein said first set of pointers comprises a read pointer, a write pointer, and a retire pointer where said read and write pointers are set apart by a fixed distance and move in unison, at all times, up and down said structure.

5. (Previously Presented) The method of claim 2, wherein said second set of pointers comprises a read pointer, a write now pointer, and a retire pointer where said read and write pointers are set apart by a fixed distance and move in unison, at all times, up and down said structure.

6. (Previously Presented) The method of claim 4, wherein said read pointer of said first set of pointers indicates said physical register location awaiting said register allocation as ~~a~~ said destination operand to identify where data should be written when said instruction of said first thread is executed by said microprocessor.

7. (Previously Presented) The method of claim 4, wherein said write pointer of said first set of pointers indicates said physical register location of said register allocated as said destination operand to identify where data should be written for said instruction of said first thread that committed.

8. (Previously Presented) The method of claim 4, wherein said retire pointer of said first set of pointers indicates said physical register location of said register allocated as said destination operand for said instruction of said thread that is next to be retired.

9. (Previously Presented) The method of claim 5, wherein said read pointer of said second set of pointers indicates said physical register location awaiting said register allocation as said destination operand to identify where data should be written when said instruction of said second thread is executed by said microprocessor.

10. (Previously Presented) The method of claim 5, wherein said write pointer of said second set of pointers indicates said physical register location of said register allocated as said destination operand to identify where data should be written for said instruction of said second thread that committed.

11. (Previously Presented) The method of claim 5, wherein said retire pointer of said second set of pointers indicates said physical register location of said register allocated as said destination operand for said instruction of said second thread that is next to be retired.

12. (Previously Presented) The method of claim 4, wherein the number of physical register pointers between said read pointer and said retire pointer of said first set of pointers indicates said physical registers available for said register allocation for said first thread of said microprocessor.

13. (Original) The method of claim 5, wherein the number of physical register pointers between said read pointer and said retire pointer of said second set of pointers indicates said physical registers available for said register allocation for said second thread of said microprocessor.

14. (Previously Presented) The method of claim 4, wherein the number of physical register pointers between said retire pointer and said write pointer of said first set of pointers indicates said registers allocated to said destination operand for a plurality of instructions of said first thread that are to become available for reallocation upon retirement of said plurality of instructions.

15. (Original) The method of claim 5, wherein the number of physical register pointers between said retire pointer and said write pointer of said second set of pointers indicates said physical registers allocated to said destination operand for a plurality of instructions of said second thread that are to become available for reallocation upon retirement of said plurality of instructions.

16. (Previously Presented) The method of claim 4, wherein said register allocated for said plurality of instructions of said first thread of said microprocessor that have not yet committed is defined by the number of physical register pointers bounded by said read pointer and said retire pointer minus said fixed distance between said read pointer and said write pointer of said first set of pointers.

17. (Previously Presented) The method of claim 5, wherein said register allocated for said plurality of instructions of said second thread of said microprocessor that have not yet committed is defined by the number of physical register pointers bounded by said read pointer and said retire pointer minus said fixed distance between said read pointer and said write pointer of said second set of pointers.

18. (Original) The method of claim 1, wherein said method of register allocation is performed in a modulo-8 memory array.

19. (Previously Presented) The method of claim 16, further comprising the step of restoring said register allocated for said instruction of said first thread of said microprocessor that has not yet committed to its previous state in said first thread of said microprocessor by pointing said read pointer of said first set of pointers to said physical register pointer allocated to said physical register location corresponding to said instruction being flushed by said microprocessor.

20. (Previously Presented) The method of claim 17, further comprising the step of restoring said register allocated for said instruction of said second thread of said microprocessor that has not yet committed to its previous state in said second thread of said microprocessor by pointing said read pointer of said second set of pointers to said physical register pointer allocated to said physical register location corresponding to said instruction being flushed by said microprocessor.

21. (Previously Presented) In a multithreading microprocessor performing speculative instruction execution, a method comprising the steps of:

providing a single structure to track register allocation for a first thread and a second thread of said multithreading microprocessor;

tracking a first set of pointers in said structure assigned to manage said register allocation for an instruction of said first thread of said multithreading processor to prevent a register allocated as a destination operand for said instruction of said first thread from being overwritten before said instruction of said first thread retires; and

tracking a second set of pointers in said structure assigned to manage said register allocation for an instruction of said second thread of said multithreading processor to prevent a register allocated as a destination operand for said instruction of said second thread from being overwritten before said instruction of said second thread retires, whereby said first set of pointers and said second set of pointers track independently of each other.

22. (Previously Presented) A semiconductor device having a plurality of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out-of-order execution, comprising:

a first module providing a structure for holding information identifying available physical registers for said microprocessor;

a first set of register pointers assigned to a first portion of said structure to track said physical registers assigned as said destination registers for a first thread of said microprocessor, said first set of register pointers includes a retire row pointer to identify where a pointer pointing to at least one of said plurality of physical registers assigned as a destination register for an instruction in said first thread that is next to be retired and a read pointer to identify where a pointer pointing to an available physical register available for assignment as a destination operand for an instruction for said first thread, wherein when said microprocessor issues a flush request for said instruction in said first thread, moving said read pointer of said first set of register pointers to said physical register assigned as said destination register for said instruction being flushed in said first thread to restore said physical register to a previous state.

23. (Original) The semiconductor device of claim 22, further comprising a second set of register pointers assigned to a second portion of said structure to track said physical registers assigned as said destination registers for a second thread of said microprocessor and when said microprocessor issues a flush request for an instruction in said second thread, moving a read pointer of said second

set of register pointers to said physical register assigned as said destination register for said instruction being flushed in said second thread to restore said physical register to a previous state.

24. (Original) The semiconductor device of claim 22, wherein said structure comprises a free physical register list for said identification of said available physical requests for said microprocessor.

25. (Previously Presented) The semiconductor device of claim 23, wherein said first set of register pointers move independently of said second set of register pointers, wherein said first set of register pointers identify said physical registers assigned to instructions in said first thread of said microprocessor that have not been committed and said second set of register pointers identify said physical registers assigned to instructions in said second thread of said microprocessor that have not been committed.

26. (Previously Presented) The semiconductor device of claim 22, wherein said first set of register pointers further comprises, a write row pointer, wherein said write row pointer identifies where a pointer pointing to said physical register of an instruction in said first thread should be written when said instruction commits.

27. (Previously Presented) The semiconductor device of claim 23, wherein said second set of register pointers further comprises, a write row pointer and a retire row pointer, wherein said write row pointer identifies where a pointer pointing to said physical register of an instruction in said second thread that is committed should be written, and said retire row pointer identifies where a pointer pointing to said physical register of an instruction in said second thread that is next to be retired.

28. (Original) A semiconductor device having a plurality of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out-of-order execution, comprising:

a first module providing a structure for holding information identifying available physical registers for said microprocessor;

a first set of register pointers assigned to a first portion of said structure to track said physical registers assigned as said destination registers for a first thread of said microprocessor and when said microprocessor issues a flush request for an instruction in said first thread, moving a read pointer of said first set of register pointers to said physical register assigned as said destination register for said instruction being flushed in said first thread to restore said physical register to a previous state; and

a second set of register pointers assigned to a second portion of said structure to track said physical registers assigned as said destination registers for a second thread of said microprocessor and when said microprocessor issues a flush request for an instruction in said second thread, moving a read pointer of said second set of register pointers to said physical register assigned as said destination register for said instruction being flushed in said second thread to restore said physical register to a previous state.

29. (Previously Presented) A computer readable medium holding computer executable instructions for performing a method in a microprocessor performing speculative instruction execution, said method comprising the steps of:

providing a structure to track register allocation for a first thread of said microprocessor; and

tracking a first set of pointers in said structure assigned to manage said register allocation for an instruction of said first thread of said microprocessor to prevent a register allocated as a destination operand for said instruction of said first thread from being overwritten before said instruction of said first thread retires, said first set of pointers includes a first pointer and a second pointer always set apart by a fixed distance and move in unison, at all times, up and down said structure.

30. (Previously Presented) The computer readable medium of claim 29 further comprising the step of tracking a second set of pointers in said structure assigned to manage said register allocation for an instruction of a second thread of said microprocessor to prevent a register allocated as a destination operand for said instruction of said second thread from being overwritten before said instruction of said second thread retires, whereby said first set of pointers and said second set of pointers track independently of each other.

31. (Previously Presented) The computer readable medium of claim 29, wherein said structure comprises pointers to said registers allocated and pointers to registers deallocated, where said registers allocated and said registers deallocated are physical registers that operate as a destination operands for said instruction of said first thread executing on said microprocessor where said destination operands identifies where data resulting from logical operations are to be written.

32. (Previously Presented) The computer readable medium of claim 29, wherein said first set of pointers further comprises a read pointer, a write pointer, and a retire pointer wherein said read pointer and said write pointer are set apart by a fixed distance and move in unison, at all times, up and down said structure.

33. (Previously Presented) The computer readable medium of claim 30, wherein said second set of pointers comprises a read pointer, a write pointer, and a retire pointer wherein said read pointer and said write pointer are set apart by a fixed distance and move in unison, at all times, up and down said structure.

34. (Previously Presented) The computer readable medium of claim 32, wherein said read pointer of said first set of pointers indicates said physical register location awaiting said register allocation as said destination operand to identify where data should be written when said instruction of said first thread is executed by said microprocessor.

35. (Previously Presented) The computer readable medium of claim 32, wherein said write pointer of said first set of pointers indicates said physical register location of said register allocated as ~~a~~ said destination operand to identify where data should be written for said instruction of said first thread that committed.

36. (Previously Presented) The computer readable medium of claim 32, wherein said retire pointer of said first set of pointers indicates said physical register location of said register allocated as ~~a~~ said destination operand for said instruction of said first thread that is next to be retired.

37. (Previously Presented) The computer readable medium of claim 33, wherein said read pointer indicates said physical register location awaiting said register allocation as said destination operand to identify where data should be written when said instruction of said second thread is executed by said microprocessor.

38. (Previously Presented) The computer readable medium of claim 33, wherein said write pointer of said first set of pointers indicates said physical register location of said register allocated as a said destination operand to identify where data should be written for said instruction of said second thread that committed.

39. (Previously Presented) The computer readable medium of claim 33, wherein said retire pointer of said first set of pointers indicates said physical register location of said register allocated as ~~a~~ said destination operand for said instruction of said second thread that is next to be retired.

40. (Original) The computer readable medium of claim 32, wherein the number of physical register pointers between said read pointer and said retire pointer of said first set of pointers indicates said physical registers available for said register allocation for said first thread of said microprocessor.

41. (Previously Presented) The computer readable medium of claim 33, wherein the number of physical register pointers between said read pointer and said retire pointer of said second set of

pointers indicates said physical registers available for said register allocation for said second thread of said microprocessor.

42. (Original) The computer readable medium of claim 32, wherein the number of physical register pointers between said retire pointer and said write pointer of said first set of pointers indicates said registers allocated to said destination operand for a plurality of instructions of said first thread that are to become available for reallocation upon retirement of said plurality of instructions.

43. (Previously Presented) The computer readable medium of claim 33, wherein the number of physical register pointers between said retire pointer and said write pointer of said second set of pointers indicates said physical registers allocated to said destination operand for a plurality of instructions of said second thread that are to become available for reallocation upon retirement of said plurality of instructions.

44. (Previously Presented) The computer readable medium of claim 32, wherein said register allocated for said instructions of said first thread of said microprocessor that have not yet committed is defined by the number of physical register pointers bounded by said read pointer and said retire pointer minus said fixed distance between said read pointer and said write pointer of said first set of pointers.

45. (Previously Presented) The computer readable medium of claim 33, wherein said register allocated for said instructions said second thread of said microprocessor that have not yet committed is defined by the number of physical register pointers bounded by said read pointer and said retire pointer minus said fixed distance between said read pointer and said write pointer of said second set of pointers.

46. (Original) The computer readable medium of claim 29, wherein said method of register allocation is performed in a modulo-8 memory array.

47. (Previously Presented) The computer readable medium of claim 44, further comprising the step of restoring said register allocated for said instruction of said first thread of said microprocessor that has not yet committed to its previous state in said first thread of said microprocessor by pointing said read pointer of said first set of pointers to said physical register pointer allocated to said physical register location corresponding to said instruction being flushed by said microprocessor.

48. (Previously Presented) The computer readable medium of claim 45, further comprising the step of restoring said register allocated for said instruction of said second thread of said microprocessor that has not yet committed to its previous state in said second thread of said microprocessor by pointing said read pointer of said second set of pointers to said physical register pointer allocated to said physical register location corresponding to said instruction being flushed by said microprocessor.

49. (Previously Presented) A computer readable medium holding computer executable instructions for performing a method in a multithreading microprocessor performing speculative instruction execution, said method comprising the steps of:

providing a single structure to track register allocation for a first thread and a second thread of said multithreading microprocessor;

tracking a first set of pointers in said structure assigned to manage said register allocation for an instruction of said first thread of said multithreading processor to prevent a register allocated as a destination operand for said instruction of said first thread from being overwritten before said instruction of said first thread retires; and

tracking a second set of pointers in said structure assigned to manage said register allocation for an instruction of said second thread of said multithreading processor to prevent a

register allocated as a destination operand for said instruction of said second thread from being overwritten before said instruction of said second thread retires, whereby said first set of pointers and said second set of pointers track independently of each other.

50. (Previously Presented) The method of Claim 21, wherein the single structure includes at least one protected register region identifying physical register pointers allocated to instructions having a logical destination register decoded and issued but not yet retired.